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Date: June 24, 2003

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Masahiko KAWASE et al.	Art Unit: 2813
Serial No.: 10/090,806	Examiner: N. O. Berezny
Filed: March 6, 2002	
Title: A CHIP-TYPE COMPOSITE ELECTRONIC COMPONENT AND MANUFACTURING METHOD THEREOF	

INFORMATION DISCLOSURE STATEMENT

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Pursuant to 37 C.F.R. § 1.56, submitted herewith are copies of four (4) references cited in the enclosed Examination Report issued in a corresponding Japanese patent application. For the Examiner's convenience, we have enclosed an English translation of the Japanese Examination Report from the corresponding Japanese Patent Application and a completed Form PTO-1449. The statement is not a representation that all of the information cited is necessarily effective as prior art against the application.

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I hereby state that each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application not more than 3 months prior to the filing of this statement, and that this is the first citation of these prior art references by a foreign patent office in a counterpart foreign patent application. Accordingly, no fee is necessary for the filing of this statement. Should the Commissioner determine otherwise, the Commissioner is authorized to charge Deposit Account No. 50-1353 for any fee shortages, including the petition fee under 37 C.F.R. § 1.17(p).

Applicants respectfully request that the disclosed references be made of record in the subject application.

Respectfully submitted,



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